

STY60NM60

N-CHANNEL 600V - 0.050Ω - 60A Max247 Zener-Protected MDmesh™Power MOSFET

| TYPE | V _{DSS} | R _{DS(on)} | I _D |
|-----------|------------------|---------------------|----------------|
| STY60NM60 | 600V | < 0.055Ω | 60 A |

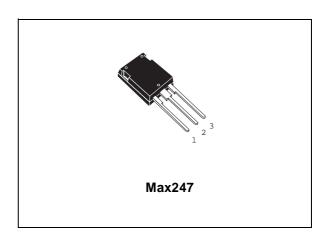
- TYPICAL $R_{DS}(on) = 0.050\Omega$
- HIGH dv/dt AND AVALANCHE CAPABILITIES
- IMPROVED ESD CAPABILITY
- LOW INPUT CAPACITANCE AND GATE CHARGE
- LOW GATE INPUT RESISTANCE
- TIGHT PROCESS CONTROL
- INDUSTRY'S LOWEST ON-RESISTANCE

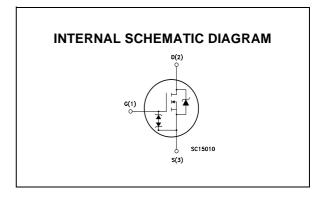


The MDmesh™ is a new revolutionary MOSFET technology that associates the Multiple Drain process with the Company's PowerMESH™ horizontal layout. The resulting product has an outstanding low on-resistance, impressively high dv/dt and excellent avalanche characteristics. The adoption of the Company's proprietary strip technique yields overall dynamic performance that is significantly better than that of similar competition's products.



The MDmesh™ family is very suitable for increasing power density of high voltage converters allowing system miniaturization and higher efficiencies.





ORDERING INFORMATION

| SALES TYPE | MARKING | PACKAGE | PACKAGING |
|------------|---------|---------|-----------|
| STY60NM60 | Y60NM60 | Max247 | TUBE |

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ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|-----------------------|--|------------|------|
| V_{DS} | Drain-source Voltage (V _{GS} = 0) | 600 | V |
| V_{DGR} | Drain-gate Voltage ($R_{GS} = 20 \text{ k}\Omega$) | 600 | V |
| V _{GS} | Gate- source Voltage | ±30 | V |
| I _D | Drain Current (continuous) at T _C = 25°C | 60 | А |
| ID | Drain Current (continuous) at T _C = 100°C | 37.8 | Α |
| I _{DM} (•) | Drain Current (pulsed) | 240 | Α |
| P _{TOT} | Total Dissipation at T _C = 25°C | 560 | W |
| V _{ESD(G-S)} | Gate source ESD(HBM-C=100pF, R=15KΩ) | 6 | KV |
| | Derating Factor | 4.5 | W/°C |
| dv/dt (1) | Peak Diode Recovery voltage slope | 15 | V/ns |
| T _{stg} | Storage Temperature | -65 to 150 | °C |
| Tj | Max. Operating Junction Temperature | 150 | °C |

^(•)Pulse width limited by safe operating area

THERMAL DATA

| Rthj-case | Thermal Resistance Junction-case | Max | 0.22 | °C/W |
|----------------|--|---------|------|------|
| Rthj-amb | Thermal Resistance Junction-ambient | Max | 30 | °C/W |
| T _I | Maximum Lead Temperature For Soldering | Purpose | 300 | °C |

AVALANCHE CHARACTERISTICS

| Symbol | Parameter | Max Value | Unit |
|-----------------|--|-----------|------|
| I _{AR} | Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max) | 30 | Α |
| E _{AS} | Single Pulse Avalanche Energy (starting $T_j = 25$ °C, $I_D = I_{AR}$, $V_{DD} = 35$ V) | 1.4 | J |

GATE-SOURCE ZENER DIODE

| Symbol | Parameter | Test Conditions | Min. | Тур. | Max. | Unit |
|------------|----------------------------------|------------------------|------|------|------|------|
| BV_{GSO} | Gate-Source Breakdown Voltage | Igs=± 1mA (Open Drain) | 30 | | | V |

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

⁽¹⁾ $I_{SD} \leq 60A$, $di/dt \leq 400 A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$.

ELECTRICAL CHARACTERISTICS ($T_{CASE} = 25~^{\circ}C$ UNLESS OTHERWISE SPECIFIED) ON/OFF

| Symbol | Parameter | Test Conditions | Min. | Тур. | Max. | Unit |
|----------------------|--|--|------|-------|-------|------|
| V _{(BR)DSS} | Drain-source Breakdown Voltage | $I_D = 250 \mu A, V_{GS} = 0$ | 600 | | | V |
| I _{DSS} | Zero Gate Voltage | V _{DS} = Max Rating | | | 10 | μA |
| | Drain Current (V _{GS} = 0) | V _{DS} = Max Rating, T _C = 125°C | | | 100 | μΑ |
| I _{GSS} | Gate-body Leakage Current (V _{DS} = 0) | V _{GS} = ± 20V | | | ±10 | μΑ |
| V _{GS(th)} | Gate Threshold Voltage | $V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$ | 3 | 4 | 5 | V |
| R _{DS(on)} | Static Drain-source On Resistance | V _{GS} = 10 V, I _D = 30 A | | 0.050 | 0.055 | Ω |

DYNAMIC

| Symbol | Parameter | Test Conditions | Min. | Тур. | Max. | Unit |
|--|---|--|------|--------------------|------|----------------|
| g _{fs} (1) | Forward Transconductance | $V_{DS} = I_{D(on)} \times R_{DS(on)max},$ $I_{D} = 30 \text{ A}$ | | 35 | | S |
| C _{iss} C _{oss} C _{rss} | Input Capacitance Output Capacitance Reverse Transfer Capacitance | $V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}, V_{GS} = 0$ | | 7300 2000 40 | | pF pF pF |
| R _G | Gate Input Resistance | f=1 MHz Gate DC Bias = 0 Test Signal Level = 20mV Open Drain | | 1.8 | | Ω |

SWITCHING ON

| Symbol | Parameter | Test Conditions | Min. | Тур. | Max. | Unit |
|--|--|---|------|-------------------|------|----------------|
| t _{d(on)} t _r | Turn-on Delay Time Rise Time | $V_{DD} = 300 \text{ V}, I_D = 30 \text{ A}$ $R_G = 4.7\Omega \text{ V}_{GS} = 10 \text{ V}$ (see test circuit, Figure 3) | | 55 95 | | ns ns |
| Q _g Q _{gs} Q _{gd} | Total Gate Charge Gate-Source Charge Gate-Drain Charge | $V_{DD} = 470 \text{ V}, I_D = 60 \text{ A}, V_{GS} = 10 \text{ V}$ | | 178 44.5 95 | 266 | nC nC nC |

SWITCHING OFF

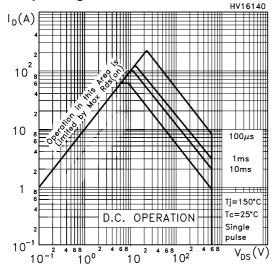
| Symbol | Parameter | Test Conditions | Min. | Тур. | Max. | Unit |
|----------------|-----------------------|---|------|------|------|------|
| $t_{r(Voff)}$ | Off-voltage Rise Time | $V_{DD} = 400 \text{ V}, I_{D} = 60 \text{ A},$ | | 130 | | ns |
| t _f | Fall Time | $R_G = 4.7\Omega, V_{GS} = 10 \text{ V}$ | | 76 | | ns |
| t _c | Cross-over Time | (see test circuit, Figure 5) | | 105 | | ns |

SOURCE DRAIN DIODE

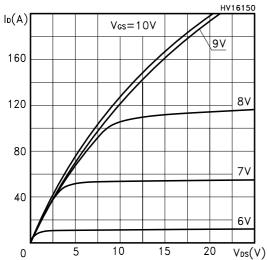
| Symbol | Parameter | Test Conditions | Min. | Тур. | Max. | Unit |
|--|--|--|------|-----------------|-----------|---------------|
| I _{SD} I _{SDM} (2) | Source-drain Current Source-drain Current (pulsed) | | | | 60 240 | A A |
| V _{SD} (1) | Forward On Voltage | $I_{SD} = 60 \text{ A}, V_{GS} = 0$ | | | 1.5 | V |
| t _{rr} Q _{rr} I _{RRM} | Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current | I_{SD} = 60 A, di/dt = 100 A/ μ s, V_{DD} = 30 V, T_j = 150°C (see test circuit, Figure 5) | | 600 14 48 | | ns µC A |

Note: 1. Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

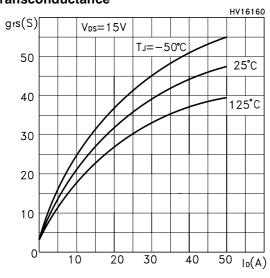
Safe Operating Area



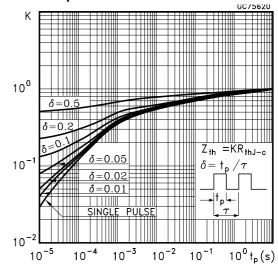
Output Characteristics



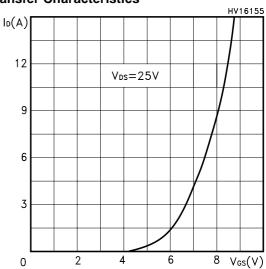
Transconductance



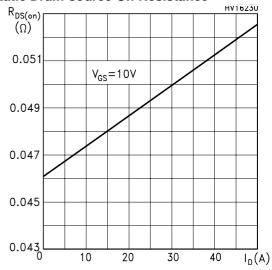
Thermal Impedance



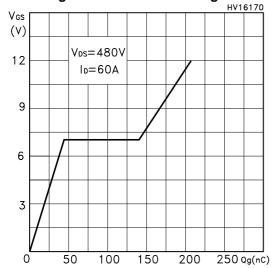
Transfer Characteristics



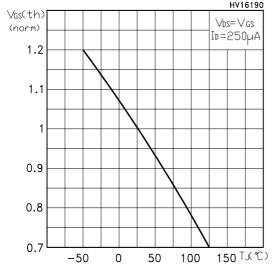
Static Drain-source On Resistance



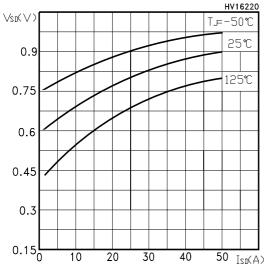
Gate Charge vs Gate-source Voltage



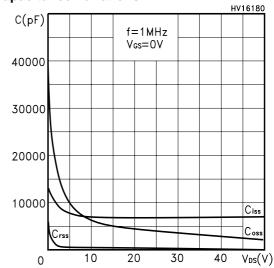
Normalized Gate Threshold Voltage vs Temp.



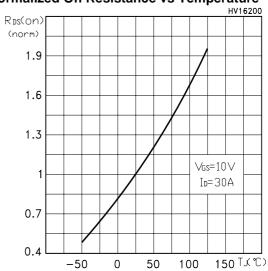
Source-drain Diode Forward Characteristics



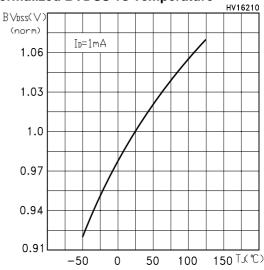
Capacitance Variations



Normalized On Resistance vs Temperature



Normalized BVDSS vs Temperature



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Fig. 1: Unclamped Inductive Load Test Circuit

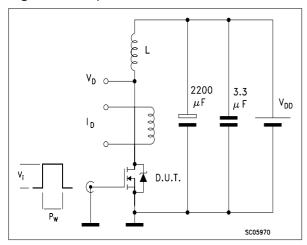


Fig. 3: Switching Times Test Circuit For Resistive Load

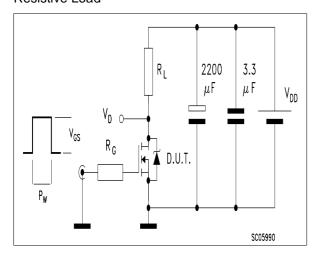


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times

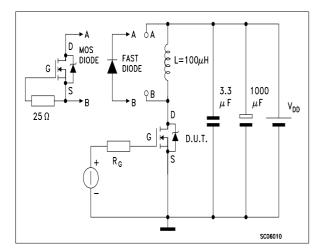


Fig. 2: Unclamped Inductive Waveform

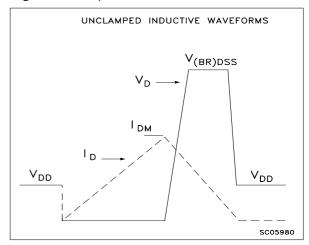
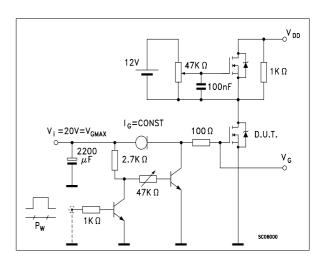
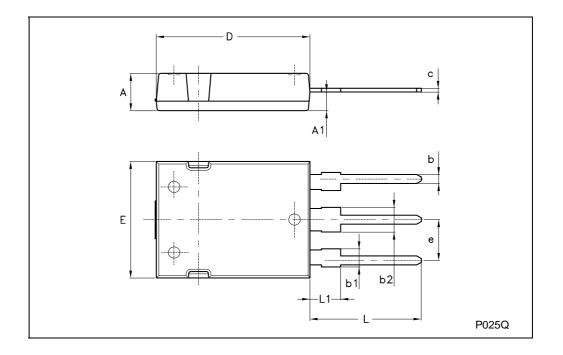


Fig. 4: Gate Charge test Circuit



Max247 MECHANICAL DATA

| DIM. | | mm | | | inch | | |
|--------|-------|------|-------|------|------|------|--|
| Dilvi. | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. | |
| Α | 4.70 | | 5.30 | | | | |
| A1 | 2.20 | | 2.60 | | | | |
| b | 1.00 | | 1.40 | | | | |
| b1 | 2.00 | | 2.40 | | | | |
| b2 | 3.00 | | 3.40 | | | | |
| С | 0.40 | | 0.80 | | | | |
| D | 19.70 | | 20.30 | | | | |
| е | 5.35 | | 5.55 | | | | |
| Е | 15.30 | | 15.90 | | | | |
| L | 14.20 | | 15.20 | | | | |
| L1 | 3.70 | · | 4.30 | | | | |



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